Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A packaged integrated circuit (IC) device comprising:

a first package part having a top surface and a bottom surface, said top and bottom surfaces having pads for I/O terminals, said first part having connector lines between terminals on said top surface and terminals on said bottom surface;

a cavity in said first package part;

a chip mounted in said cavity, said chip having an active surface including an IC and contact pads;

a second package part having a top surface and a bottom surface, said bottom surface having a first plurality of I/O terminals aligned with said chip contact pads, and a second plurality of I/O terminals aligned with said top surface I/O terminals of said first package part;

said second package part further having connector lines between said first and second plurality of terminals; said connector lines including a signal layer, a power layer, and a ground layer, spaced by insulation of a thickness between 10 and 50 μm, and formed into lines having a width less than three times said insulator thickness; and

interconnection elements between said chip contact pads and said first plurality of terminals of said second package part, and between said second plurality of terminals of said second package part and said top surface terminals of said first package part.

2. (canceled).

3. (original) The device according to Claim 1 wherein said connector lines in said second package part comprise a signal/power layer and a ground layer, said layers spaced by insulation of a thickness between 10 and 50 μmm, and formed into lines having a width less than three times said insulator thickness.

4. (original) The device according to Claim 1 wherein said chip contact pads are spaced apart by less than 100 μm, center to center.

5. (original) The device according to Claim 1 wherein said interconnection elements between said peripheral chip contact pads and said first plurality of terminals of said second package part are stud bumps.

6. (original) The device according to Claim 5 wherein said stud bumps are selected from a group consisting of gold, copper, copper/nickel/palladium, and alloys thereof.

7. (original) The device according to Claim 1 wherein said interconnection elements between said second plurality of terminals of said second part and said top surface terminals of said first part are reflow interconnections.

8. (original) The device according to Claim 7 wherein said reflow interconnections are made of a material selected from a group consisting of tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, indium, conductive adhesives, and z-axis conductives.

9. (original) The device according to Claim 1 further comprising interconnection elements attached to said bottom surface terminals of said first package part, operable to connect to external parts.

10. (original) The device according to Claim 1 wherein said chip has central contact pads as well as peripheral contact pads.

11. (original) The device according to Claim 10 wherein said second package part further comprises an opening sized to expose said central chip contact pads, and I/O terminals distributed around said opening, said terminals on said top surface.

12. (original) The device according to Claim 10 wherein said first plurality of bottom I/O terminals of the second package part is aligned with said peripheral chip contact pads.

13. (original) The device according to Claim 10 wherein bonding wires connect said central chip contact pads and said top surface terminals of said second package part.

14. (original) The device according to Claim 10 wherein interconnection elements connect said peripheral chip contact pads and said first plurality of terminals of said second package part, and said second plurality of terminals of said second package part and said top surface terminals of said first package part.

15. (original) The device according to Claim 13 further comprising encapsulation material covering said bonding wires and at least portion of said second package part and of said chip.

16. (currently amended) A packaged integrated circuit (IC) device comprising:

a first package part having a top surface and a bottom surface, said top and bottom surfaces having pads for I/O terminals, said first part having connector lines between terminals on said top surface and terminals on said bottom surface;

a chip mounted on said top surface of said first package part, said chip having an active surface including an IC and contact pads;

a second package part having a top surface and a bottom surface, said bottom surface having a first plurality of I/O terminals aligned with said chip contact pads, and a second plurality of I/O terminals aligned with said top surface I/O terminals of said first package part;

said second package part further having connector lines between said first and second plurality of terminals, <u>including a signal layer, a power layer, and a ground layer, spaced by insulation of a thickness between 10 and 50 μm, and formed into lines having a width less than three times said insulator thickness</u>; and

interconnection elements between said chip contact pads and said first plurality of terminals of said second package part, and between said second plurality of terminals of said second package part and said top surface terminals of said first package part.

26. (original) The device according to Claim 25 wherein said second package part further comprises an opening sized to expose said central chip contact pads, and I/O terminals distributed around said opening, said terminals on said top surface.

27. (original) The device according to Claim 25 wherein said first plurality of bottom I/O terminals of the second package part is aligned with said peripheral chip contact pads.

28. (original) The device according to Claim 25 wherein bonding wires connect said central chip contact pads and said top surface terminals of said second package part.

29. (original) The device according to Claim 25 wherein interconnection elements connect said peripheral chip contact pads and said first plurality of terminals of said second package part, and said second plurality of terminals of said second package part and said top surface terminals of said first package part.

30. (original) The device according to Claim 25 further comprising encapsulation material covering said bonding wires and at least portion of said second package part and of said chip.

31 – 41. (canceled)